

I claim:

- 1 1. A system comprising:  
 2 a processor; and  
 3 a memory device coupled to the processor, the memory device including:  
 4 a main memory; and  
 5 a cache memory coupled to the processor and to the main memory to  
 6 increase effective access speed between the processor and the  
 7 memory device.
- 1 2. The system of claim 1, wherein:  
 2 the cache memory and main memory are on a same integrated circuit.
- 1 3. The system of claim 1, wherein:  
 2 the main memory is a flash memory.
- 1 4. The system of claim 1, wherein:  
 2 the cache memory can hold no more than sixteen addresses at the same time.
- 1 5. The system of claim 1, wherein:  
 2 the cache memory, main memory, and processor are on a same integrated  
 3 circuit.

1 6. An apparatus comprising:  
2 a memory device to couple to a processor through a bus, the memory device  
3 including:  
4 a main memory; and  
5 a cache memory coupled to the main memory to increase effective  
6 access speed between the processor and the memory device.

1 7. The apparatus of claim 6, wherein:  
2 the cache memory is on a same integrated circuit as the main memory.

1 8. The apparatus of claim 6, wherein:  
2 the main memory is a flash memory.

1 9. The apparatus of claim 6, wherein:  
2 the cache memory can hold no more than sixteen addresses at one time.

1 ~~10. A method, comprising:~~  
2 ~~requesting data from an address of a main memory;~~  
3 ~~determining if the address is contained in a cache memory located on a same~~  
4 ~~integrated circuit with the main memory;~~  
5 ~~retrieving the data from the cache memory if the address is contained in the~~  
6 ~~cache memory;~~  
7 ~~retrieving the data from the main memory if the address is not contained in the~~  
8 ~~cache memory; and~~  
9 ~~providing the retrieved data to a requester.~~

1 11. The method of claim 10, further comprising:  
 2 if determining determines that the address is not contained in the cache  
 3 memory, placing the data and the address into the cache memory.

1 12. The method of claim 10, wherein:  
 2 retrieving the data from main memory includes retrieving a quadword  
 3 containing the data.

1 13. The method of claim 10, wherein:  
 2 retrieving the data from cache memory includes retrieving a quadword  
 3 containing the data.

1 14. The method of claim 10, wherein:  
 2 the cache memory includes no more than sixteen locations for storing data.

1 15. The method of claim 10, wherein:  
 2 requesting data from a main memory includes requesting data from a flash  
 3 memory.

1 16. A method, comprising:  
 2 requesting data from a plurality of sequential addresses of a main memory in a  
 3 burst transfer;  
 4 determining if the addresses are contained in a cache memory located on a same  
 5 integrated circuit with the main memory;

6 if the addresses are contained in the cache memory, retrieving the data from the  
 7 cache memory;  
 8 if the addresses are not contained in the cache memory, retrieving the data from  
 9 the main memory, and placing the data and at least one of the addresses  
 10 into the cache memory;  
 11 initiating a transfer of the requested data to a requester;  
 12 interrupting the transfer after transferring a first portion of the requested data;  
 13 and  
 14 resuming the transfer by retrieving a second portion of the requested data from  
 15 the cache memory and transferring the second portion to the requester.

1 17. The method of claim 16, wherein:  
 2 retrieving the data from main memory includes retrieving a quadword  
 3 containing the data.

1 18. The method of claim 16, wherein:  
 2 retrieving the data from cache memory includes retrieving a quadword  
 3 containing the data.

1 19. The method of claim 16, wherein:  
 2 requesting data from a main memory includes requesting data from a flash  
 3 memory.

1 20. The method of claim 16, wherein:  
 2 the cache memory includes no more than sixteen locations for storing data.